Abstract—A capacitorless multi-voltage domain analog low dropout (LDO) regulator is presented in this paper. The low dropout regulator is designed with a 1.5 V supply voltage and tends to regulate four voltage domains between 0.8 V and 1.4 V based on user’s input selection. At a heavy load, the LDO consumes only 52.88 µA of quiescent current while preserving a current efficiency of 99.98%. The proposed LDO has been designed on a 0.18-µm CMOS process with an area of 0.149 mm² and supply current capacities up to 400 mA. The line and load regulation of the proposed regulator is 1.85 mV/V and 0.0003 mV/mA for lower output voltage and 3.53 mV/V and 0.079 mV/mA at higher output voltage respectively. During the standby mode, the LDO only consumes 174.5 µW which is relatively low. The LDO is suitable for use in embedded system applications because no external component is needed for powering it up.

Keywords—Low Dropout, LDO, Power Management Unit, PMU, Bandgap voltage reference, BGR, System on Chip, SoC, Internet of things, IoT

I. INTRODUCTION

Multi-voltage domain is commonly employed in electrical systems to enable fine-grained power delivery. In system on chip, SoC, power management unit was used to regulate the multi-voltage domain to power up the various load circuits [1]. Same as goes to devices on the Internet of Things, IoT application. Sensors, a processing unit, and an RF transceiver are the blocks typically used in Internet-of-Things (IoT) applications ranging from wearables to environmental monitoring powered up with multi-voltage domain [2]. Apart from this, device level application, such as a Field Programmable Gate Arrays (FPGA) or Complex Programmable Logic Device (CPLD) devices, more than one voltage domain is required to power up. Even though power management unit (PMU) could be a good solution for multi-voltage domain, for some IoT application, the infrequent monitoring, such as remote patient heart-rate monitoring or industrial temperature sensing, the wireless sensor in idle state with correspondingly less time in active mode.

Besides the PMU, a single-inductor multiple-output (SIMO) dc-dc converter could be another alternative for multi-voltage domain. Multiple independent dc-dc converters were replaced with SIMO dc-dc converters, which have a single inductor and can regulate multiple voltages while maintaining high power efficiency. However, switching noise and cross regulation were limiting this solution from being used in an embedded system [3]. Multiple independent LDO without switching noise are ideal for embedded system applications as LDO may offer clean power with little ripples[4]. In embedded applications such as biomedical systems that demand high efficiency, low ripple, low electromagnetic interference (EMI), and low interference, multiple independent regulated voltages are required [5]. Guo, et al. developed an architecture that stacks a main LDO and many auxiliary push pull regulators (APPRs) to generate several voltages for varied loads in a single SoC chip, hence avoiding cross regulation [6]. However, the LDO only can support a light load and relatively larger chip area.

Digital LDO is prominent solution for the multiple voltage domain architecture due to their dynamic voltage scaling and intrinsic characteristics of discontinuous-time control. Since, the control signal from digital controller on the DLD0 only refresh at the edge of the clock and hold on until next clock cycle, the controller in the DLDO is under utilized [7]. The time division multiplexing technique is great effort to
regulate the multiple voltage domain from the digital controller. 

Lu et al. proposed single controller multiple output DLDO with four pass devices integrated with intention to regulate four output voltage [7]. To enhance the DLDO’s transient response, a high clock frequency and a push-pull auxiliary loop (PPAloop) were used. As a power-saving measure, the clock will be frozen during the steady-state condition, and analog-assisted loop will take over control. However, this solution required relatively higher silicon area as various digital circuit need to accommodate. Besides that, off-chip capacitors are ideal for embedded and SoC applications.

This work proposes a multi-voltage domain analog LDO without off-chip capacitor to address the aforementioned concerns. The quiescent current was optimised without compromising LDO performance in terms of line regulation, load regulation, or chip area.

II. CIRCUIT ARCHITECTURE AND APPLICATION

A. Circuit Architecture

Fig. 1 shows the circuit architecture of the multi-voltage domain LDO regulator. LDO is used to step down the supply voltage to regulate output voltage using active devices.

As a conventional LDO, this multi-voltage domain LDO regulator typically consists of an error amplifier, pass element, and feedback resistor. Error amplifier was used to correct the error at output voltage by controlling the gate voltage of the pass device when the negative feedback voltage differs from the reference voltage. The bandgap reference, BGR circuit is used to supply a reference voltage. Negative feedback is established by a resistive divider of the output voltage, feedback to the error amplifier. As a result, the output of the error amplifier is decrease when the regulated output voltage is lower than the reference voltage. When the regulated output voltage is higher than the reference voltage, the output voltage of the error amplifier is increased. In multi-voltage domain application, the lower feedback resistor, R2A, R2B, R2C, and R2D were added in order to generate more than one output voltage. Apart from that, in each path of the feedback resistor, for switching purposes, an NMOS transistor was added. The gate voltage of each NMOS transistor was controlled by a demultiplexer based on user input selection. At a time, only one output voltage can be regulated.

B. Application of Multi-domain LDO

The proposed LDO is good to use in the Embedded system design as compatibility, small size and no external component is required. Besides this, since the output voltage was able to configure using the DEMUX, the processor such as microcontroller able to configure the intended output. Fig. 2 shows a block diagram of an IoT application that employs the proposed LDO.

Since four distinct devices must be powered up with various voltage domains, the output of LDO has been connected to each device in simultaneously while the processor configured the appropriate output based on the requirements. It improves power efficiency since the device is only powered on when it is needed, and it reduces the number of LDOs while lowering the BOM cost and PCB size.

Fig. 2 shows a block diagram of proposed LDO in IoT application.
were added at bottom of feedback resistor which is $R_{2A}$, $R_{2B}$, $R_{2C}$, and $R_{2D}$. Apart from that, the NMOS transistor, $MN_A$, $MN_B$, $MN_C$, $MN_D$, on each path was added. These transistors are functioning as a switch. At a time, only one path will be active while other paths will be disable. The ratio of the feedback resistor in active path will regulate the output voltage accordingly. Simple demultiplexer design was used to control the switches and regulate the desired output voltage accordingly.

Fig. 4. shows the logic level of demultiplexer design. This demultiplexer requires three input signals to generate four output signals which control the switched-on feedback network. $A_0$, $A_1$, $A_2$, and $A_3$ are the output signal of the demultiplexer, whereas $V_A$, $V_B$, and $EN$ are the input signals.

Since the supply voltage, VDD of the LDO is 1.5 V, the voltage level of the input signal on the demultiplexer is 1.5 V. EN signal was used to turn on the LDO regulator. If the logic of EN signal were LOW, all four switches will be open, as a result, the LDO is fully turned OFF with initiative to reduce the quiescent current. For control the switches on the feedback network, $V_A$ and $V_B$ signals are taking control. The truth table of the demultiplexer shown in Table I.

The demultiplexer is designed with a smaller transistor, notably in terms of W/L, to reduce power consumption since the drain current, $I_D$, able to control with tune the ratio of W/L on transistors. Because this circuit is typically turned on all the time, the demultiplexer consumes only 10 $\mu$A and 15 $\mu$A of current in both standby and operating modes respectively. The EN signal used to switch the mode of the LDO from operating to standby mode with intended to reduce the quiescent current during idle state.

The LDO in this design, could support up to 400 mA load current. In order to support the huge current, the size of the pass transistor is a matter. PMOS transistors were employed as pass transistors in the proposed design, and they function in the saturation region. Smaller size of pass transistor can only support a modest load current, whereas larger devices can support a large current based on their maximum capacity. By increasing the size of the transistor in order to support higher load current, its impact the size of the chip and parasitic capacitance increase and degrade the stability of the system. In the proposed design, the multiple transistors were connected as parallel while the size of each transistor practically smaller. Fig. 5, depicts the proposed LDO’s pass transistor design.

The parallel pass transistor approach increases the capacity of the pass device to accommodate large load currents while keeping the transistor size in line with the size of the LDO. Simultaneously, smaller transistors require less current during operation and standby mode. As a result, the quiescent current is substantially reduced, and the LDO’s current efficiency were improved.
IV. RESULTS AND DISCUSSION

The proposed multi-voltage domain LDO regulator was designed using 180 nm CMOS process technology model and verify the feasibility of the proposed design topology through the simulation. Fig. 6 illustrates the simulated results of multi-voltage domain output voltage from 0.8 V to 1.4 V with supply voltage of 1.5 V.

The test configuration setup employed in Table II.

<table>
<thead>
<tr>
<th>V&lt;sub&gt;output&lt;/sub&gt;, V</th>
<th>V&lt;sub&gt;A&lt;/sub&gt;</th>
<th>V&lt;sub&gt;B&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>1.0</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>1.2</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>1.4</td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>

Fig. 7 demonstrates the quiescent current of the multi-voltage domain LDO during no load condition. Based on the results, the lowest quiescent current is 46.8 µA while highest is 52.9 µA with the output voltage of 0.8 V and 1.4 V respectively. Highest multi-voltage domain output voltage contributes to largest quiescent current while otherwise vice versa. The results dictate that output voltage is directly proportional to quiescent current. This quiescent current is the total operating current for bandgap reference, differential amplifier and de-multiplexer which operate during no load and full load condition.

The load regulation on the multi-voltage domains shown in Fig. 8. DC analysis was conducted to plot V<sub>output</sub> versus I<sub>load</sub> and load regulation is computed from the plotted waveform.

The load regulation for multi vol of 0.8 V, 1.0 V, 1.2 V and 1.4 V is 0.0003 mV/µA, 0.000325 mV/µA, 0.0004 mV/µA, and 0.079 mV/µA respectively.

V. CONCLUSION

A capacitorless multi-voltage domain low dropout regulator for embedded system application is proposed in this paper. The LDO can operate at 1.5 V and has a wide output range of 0.8V to 1.4V, as well as support load current up to 400 mA to each of the four output voltage domains. Furthermore, the quiescent current of LDO is 46.83 µA for lower output and 52.88 µA for higher output, which is a comparably very low current. The error amplifier design was optimized with a high DC gain, resulting in excellent load and line regulation of 0.001 mV/µA and 1.85 mV/V, respectively. With a load of 400 mA, the current efficiency was 99.98% across the entire voltage domain.

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