Performance Analysis of Junctionless Multi-Bridge Channel FET with Strained SiGe Application

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Abstract—In this work, a 12 nm 3-Dimensional (3D) strained Junctionless (JL) Multi-Bridge Channel Field Effect Transistor (MBCFET) with different Germanium (Ge) mole fractions from 0.1 to 0.4 are presented. The strain used in this work is Silicon-Germanium (SiGe) which is applied in between the channels of MBCFET. The electrical performances such as on-current, threshold voltage and potential distributions along the channel are conducted by using the Silvaco TCAD simulator. It was found that the strained JL MBCFET performs better compared to unstrained JL MBCFET. The results show that by inducing strain on JL MBCFET, the on-current increased by 29%, threshold voltage shifted by 0.25 V and potential in the centre of the channel was reduced by 13%.

Keywords—3D, Strained, Junctionless, Multi-bridge channel FET, Ge mole fractions, SiGe, TCAD

I. INTRODUCTION

Severe short-channel effect (SCE) on conventional MBCFETs owing to its physical limitation led to the introduction of new materials and structures [1]. For the device structure, it has been improved by increasing the number of junction surfaces connecting the channel and the gate. MBCFET has been proposed which consists of vertically stacked nanosheets and a Gate-All-Around (GAA) structure. This structure itself allows a maximum area of contact between channel and gate if compared to FinFETs. In particular, MBCFET has become one of the promising candidates for replacing FinFETs for the next generation transistors due to its superior gate controllability for the stacked channels.

For a conventional MBCFET, the formation of the source-drain during fabrication becomes so challenging, especially for the bottom channel [2]. The fact that a junctionless field-effect transistor (JLFET) has no junction helps in avoiding complex doping engineering. Previous device such as nanowire has implemented junctionless and proven to increase the on-current compared to conventional nanowire [3], [4]. Unfortunately, the drive current of Junctionless MBCFET is lower compared to conventional MBCFET although the doping is increased. Also, the stacked channels in MBCFET are not being fully utilized as the intensity of current density decreases moving to the second and third channels at the bottom [5]. It shows a variation of current density across the channels.

Strain engineering has received positive attention as an alternative to improve the drive current without changing the geometry dimension of the device itself. Generally, there are two types of strain namely global strain and local strain. Global strain is where strain is induced at the channel whereas a local strain is induced at the source and drain region. The forces involved in the strain are tensile and compression. Fig. 1 represents two types of global strain namely Type I and Type II. The set-up of the Silicon (Si) and SiGe layers, as well as the strain direction, differ between these two strains. For both NMOS and PMOS, type II boosted the electron and hole carriers, but type I solely improved the hole carriers for PMOS.

![Strained SiGe](image1)

**Fig. 1.** Global strain for (a) Type I and (b) Type II

Previous research has introduced strain into junctionless transistors for instance; Double-gate MOSFETs, FinFETs and Nanowires as an effort to improve electrical performances without further scaling [6]–[8]. However, there are still no reports on induced strain on the junctionless...
MBCFET as shown in Fig. 2. Therefore, analyses and investigations should be performed to determine the benefits and limitations of this device.

In this study, the strained junctionless is simulated using Atlas Silvaco TCAD and its electrical performances are studied. MBCFET with gate length of 12 nm, source-drain doping of $3 \times 10^{20}$ cm$^{-3}$, channel doping of $1 \times 10^{17}$ cm$^{-3}$ and drain source voltage of 0.65 V is simulated followed by this reference [9]. The current-voltage (I$D$–V$GS$) curve of the published data [10] and the simulated MBCFET are compared to verify the validity of the simulated structure. The strain used for this work is Si$_{1-x}$Ge$_x$, where x is the Ge mole fractions.

![Figure 2](image)

**Fig. 2.** The cross-section of strained JL MBCFET at one of the channels. Global strain is used in this work.

II. DEVICE STRUCTURES

The physical parameters of conventional MBCFET are given in Table 1. The material used for the gate is Titanium Nitride (TiN) while Silicon Nitride (Si$_3$N$_4$) is used as spacers. The metal work function of the gate is varied within 4.57 eV. The thickness of Silicon Oxide (SiO$_2$) and Hafnium Oxide (HfO$_2$) is 0.5 nm and 1.28 nm respectively. The thickness of each nanosheet, NSH$_{TH}$ is 5 nm and the width of each nanosheet, NSH$_W$ is 50 nm.

**TABLE I. PHYSICAL PARAMETERS CONSIDERED IN THIS WORK**

<table>
<thead>
<tr>
<th>Device Parameter</th>
<th>[9]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length, L$_g$</td>
<td>12 nm</td>
<td>12 nm</td>
</tr>
<tr>
<td>Source drain doping, N$_{sd}$</td>
<td>$3 \times 10^{20}$ cm$^{-3}$</td>
<td>$3 \times 10^{20}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Channel doping</td>
<td>$1 \times 10^{17}$ cm$^{-3}$</td>
<td>$1 \times 10^{17}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Source Drain Voltage, V$_{DS}$</td>
<td>0.65 V</td>
<td>0.65 V</td>
</tr>
<tr>
<td>Doping in the strain silicon layer and SiGe layer</td>
<td>–</td>
<td>$1 \times 10^{16}$ cm$^{-3}$ – $1 \times 10^{17}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Ge mole fraction in SiGe layer</td>
<td>–</td>
<td>0-40%</td>
</tr>
</tbody>
</table>

Fig. 3 depicts the cross-sectional views (a) along with (b) across the three-channel of conventional MBCFET.

![Figure 3](image)

**Fig. 3.** The simulated conventional MBCFET structures; (a) cross-sectional views of the X-Y plane (along the channel), (b) cross-sectional views of the Y-Z plane (across the channel).

For fair comparison, the I$D$–V$GS$ curve of both published work [10] is compared with this simulation work. The I$D$–V$GS$ of the simulated conventional MBCFET as shown in Fig. 4 shows a good match with fabricated MBCFET [10] which confirms the validity and reliability of this simulated MBCFET device structure. The extracted values for V$n$$_{th}$, on-current (I$on$) and subthreshold swing (SS) of [10] are 0.26 V, 1.34×$10^{-5}$ and 70.13 mV/decade respectively. Whereas the V$n$$_{th}$, on-current (I$on$) and subthreshold swing (SS) of this paper are 0.27 V, 1.32×$10^{-4}$ and 70.01 mV/decade respectively.

![Figure 4](image)

**Fig. 4.** Drain current against gate voltage (I$D$–V$GS$) characteristics of simulated conventional MBCFET compared with fabrication data (V$n$$_{th}$=0.65V).
III. STRAIN RELATED MODELS USED IN TCAD SIMULATION

Due to the strain effect, several parameters should be included such as mobility, bandgap offset and electron affinity [11], [12]. According to curve fitting in our simulation (Fig.4), the computed low mobility value for conventional MBCFET is 48 cm²/V.s. At the channel region, the mobility for strained silicon, \( \mu_b \) is defined as follow equation from [13]:

\[
m_{\text{b,Strained}} = \mu_b e^{e_{\text{ns}}} \quad (1)
\]

where \( e_{\text{ns}} \) is electron enhancement and \( \mu_b \) is the low field mobility in Silicon. The value of \( e_{\text{ns}} \) is shown in Table 2.

TABLE II. THEORETICAL PREDICTIONS OF LOW-FIELD ELECTRON AND HOLE MOBILITY ENHANCEMENTS

<table>
<thead>
<tr>
<th>Ge mole fraction, x</th>
<th>Electron enhancement, ( e_{\text{ns}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.10</td>
<td>1.46</td>
</tr>
<tr>
<td>0.20</td>
<td>1.68</td>
</tr>
<tr>
<td>0.30</td>
<td>1.70</td>
</tr>
<tr>
<td>0.40</td>
<td>1.70</td>
</tr>
</tbody>
</table>

Meanwhile, the energy changes in the conduction or valence bands are defined as bandgap offset. The bandgap offset is given by,

\[
(\Delta E_{c})_{b-Si} = 0.57x \quad (2)
\]

\[
(\Delta E_{v})_{b-Si} = 0.4x \quad (3)
\]

\[
V_T \ln \left( \frac{N_{c,\text{Si}}}{N_{V,F,\text{Si}}} \right) = V_T \ln \left( \frac{m_{\text{h,s}}}{m_{\text{h,b-Si}}} \right) \quad (4)
\]

\[
\chi_{\text{ns}} = (4.05 + 0.58x) \ V \quad (5)
\]

where \((\Delta E_{c})_{b-Si}\) is the decrease in electron affinity of silicon due to strain, \((\Delta E_{v})_{b-Si}\) decrease in the bandgap of silicon due to strain, \(x\) is the Ge mole fraction in a relaxed SiGe buffer layer.

IV. RESULTS AND DISCUSSIONS

The Id–Vds characteristics of the conventional MBCFET and the JL MBCFET which consist of 3 different n-type doping concentrations are illustrated in Fig. 5.

As can be seen, both on-current and off-current increases as the doping concentration increases. The improvement of on-current is the due to the increment of carrier mobility and reduction in ionization scattering in the channel. However, the on-current of JL MBCFET is still lower than the conventional MBCFET for all 3 different doping concentrations.

Fig. 6 shows the comparison between unstrained and strained JL MBCFET for 4 different mole fractions. After strain is induced between the channels, a significant improvement of on-current up to 28% can be observed. This proves that the low on-current in JL MBCFET now can be solved by applying strain without further downsizing the gate length which will cause other short channel effects. The lattice mismatch between the silicon and SiGe layer produces the silicon (also known as strained silicon) to be tensely stretched and increases the lattice constant which leads to the increment of on-current.

From the linear graph in Fig. 6, the threshold voltage of strained JL MBCFET is reduced by 0.25 V from the unstrained JL MBCFET. This is because the energy gap has been reduced, requiring less voltage to achieve inversion at the metal gate [14], [15]. The on-current of the unstrained JL MBCFET is 5.65x10⁻⁴ A. However, the on-current of the strained JL MBCFET are 1.6x10⁻³ A, 1.61x10⁻³ V, 1.63x10⁻³ V, 1.64x10⁻³ V for X=0.1, 0.2, 0.3, 0.4, respectively. Since the electrons get saturated for X=0.30, it is found that only a small increase in on-current as X is further increased. Saturation happens when the strain separates both conduction and valence sub-bands in energy. Consequently, the elimination of inter-valley or inter-band phonon scattering occurs virtually [16], [17].

Fig. 7 illustrates the potential distribution in the middle of the channel of unstrained and strained JL MBCFET along the channel, starting from the source to the drain. The potential distribution is plotted by taking the average potential distribution from the middle of the three channels of MBCFET. It is illustrated that the potential distribution decreases as the Ge mole fraction increases. The results indicate that the drain has more control over the channel potential for the lower value of Ge mole fraction. On the other hand, more carriers are injected through the channel by inducing higher value of mole strain. Hence, a conducting path is formed between the source and the drain. The mobility of...
the carriers is then enhanced, therefore increase the on-current of the device.

![Diagram](image.png)

**Fig. 7.** (a) The cross-sectional views of the X-Y plane of JL MBCFET (across one of the channels), showing the cut-plane (red line) of the potential distribution and (b) the potential distribution from the source to the drain of JL MBCFET and JL strained MBCFET with various Ge mole fractions, X.

V. CONCLUSION

Conventional MBCFET has been successfully simulated and validated with the experimental work. JL MBCFET and strained JL MBCFET with different Ge mole fractions are successfully simulated and presented. Based on the simulation results, it is found that strain affects the electrical performance of the devices specifically the on-current. Strained JL MBCFET with higher Ge mole strain boosts the on-current. Also, the threshold voltage is lowered with a threshold shift of 0.25V and the potential in the centre of the channel is reduced by 13%.

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