Analysis and Design of an Efficient and Wideband Common Collector Class B Amplifier for Auxiliary Envelope Tracking Supply Modulator

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Abstract—In this paper, an efficient and wideband class B amplifier is designed for the application as a supply modulator of an Envelope Tracking (ET) radio frequency power amplifier (RFPA). The common collector configuration is used to drive a low output impedance as the output signal of this amplifier will be used as the bias signal to the drain port of the RFPA. A quasi-complementary design which is also referred to as a totem-pole with a pair of n-type transistors is implemented to build the class B amplifier. In this design, the transistors are biased properly to avoid cross over distortion and thus maintain a good level of linearity. The wideband property of the amplifier has been achieved by controlling the values of the coupling capacitors. A good efficiency is recorded by using a step-up center tapped transformer at the emitter outputs of the transistors. Simulation results show that if the input AC signal level is chosen to be half of the maximum DC voltage level, then a transformer turn ratio of 1:6 will give an efficiency of 87%. Moreover, the bandwidth is recorded to be almost 80 MHz after using a 10 uF coupling capacitor of 10 uF and a 70 uF bypass capacitor. The proposed supply modulator is suitable for the base station applications of the LTE networks.

Keywords—Class B amplifier, supply modulator, envelope tracking, totem-pole, wideband, efficiency

I. INTRODUCTION

Envelope tracking (ET) offers a highly efficient power amplifier for the next generation base station and mobile UE (user equipment) applications. This technique can be thought of as a simplified version of Envelope Elimination and restoration (EER) method. The performance of an ET power amplifier largely depends on four major parameters such as linearity, efficiency, broadband and power handling capacity [1].

The design of the supply modulator is an important step which will ensure a good trade-off between maximum output power with efficiency and linearity. Supply modulators can be linear, discrete and hybrid. The linear modulators are not suitable for modern wireless communication signals of high peak to average power ratio (PAPR). These modulators are wideband and provide power at higher frequencies but have low efficiency. On the other hand, the discrete modulators are efficient and provides power to low frequencies but narrowband. Moreover, they are expensive, become lossy with the transformers and have high switching stress because of the output inversion [2-3]. The problems of linear and discrete modulators can be mitigated by combining them in series or in parallel. The series hybrid modulators are wideband, linear and highly efficient. The major problem is that it uses two stages to achieve higher efficiency which in turn requires a sufficiently high switching frequency to operate a multi stage or multi-phase modulator. On the contrary, the parallel hybrid modulator is very wideband, highly efficient and provides most power in the low-frequency range [4-6].

Another simpler variant technique of parallel hybrid topology is the Auxiliary Envelope tracking (AET) which consists of a linear supply modulator and a broadband RF transformer as a combiner. The basic difference between AET and other hybrid topology is the mechanism of generating the modulated supply. In AET, the AC and DC supply components are separated initially. The envelope signal is applied directly to the linear modulator as shown in Fig. 1. The output of the modulator is actually the AC component which will be applied to the combiner. And the DC component is supplied to the combiner from an external DC power supply. Finally, the combiner combines them to form the final AET signal. In this way, it can give easy and cost effective solutions to ET applications by offering a very simple circuit. In addition, it overcomes the challenges and efficiency issues caused by switch mode power supply modulators [7-9].

In this paper, a class B amplifier has been designed with an appropriate biasing circuit to maintain the linearity of the output AC signal. An in-house designed RF broadband transformer is used as a combiner which also suppresses the DC offset of the output AC signal. This proposed supply modulator combination of the class B amplifier and the RF broadband transformer contributes in designing a simpler,
cost effective and efficient tracking generator while maintaining a good level of linearity rather than conventional ET system.

![Fig. 1. Block diagram of AET tracking generator](image)

**II. DESIGN OF THE CLASS B AET SUPPLY MODULATOR**

The Class B AET supply modulator consists of two major components.

- Class B amplifier
- Combiner

The class B amplifier is used to produce the AET AC signal of the amplified envelope signal. In this stage, only current amplification is done. A biasing circuit is used to reduce the distortion of the output AC signal. A detailed analysis of the entire circuit of the amplifier is given below:

**A. Circuit analysis**

The class B amplifier is designed using two types of configurations which are the push-pull and the totem pole. Both use two transistors to make the conduction angle of each transistor to 180 degrees. In push-pull configuration, the bases of one npn transistor and one pnp transistor are connected together so that only one transistor is switched on at a time i.e., for the positive half cycle of the AC signal, the npn transistor is switched on and for the negative half cycle, the pnp transistor is switched on. But this configuration becomes a problem when the complementary pair of a transistor is not available. For this reason, in this research, the totem pole configuration is used where two same types of transistors are used. A phase splitter (centre tapped transformer of 1:1 ratio) is used to make two out of phase AC signals which are applied at the bases of the transistors. So, the signal cannot be switched on at the same time. Since the transistor needed to be biased to turn on at 0.55 V, there will be some portion of the AC input signal that will not pass through and cause a minimum cross-over distortion at the output AC signal. This biasing voltage can be controlled by the fixed DC supply through a voltage divider circuit. However, when the AC signal is combined to this DC biasing circuit, the resulting combined signal drops a little bit due to the clipped-off. For this reason, the value of the biasing voltage is chosen slightly more than the saturation voltage of the transistor.

For the simulation of the circuit operation, the input signal applied to this circuit is a 5 Vpp AC signal. When this AC signal source is combined with a fixed DC source via a voltage divider circuit, the AC signal will ride on a DC value depending on that voltage divider circuit. The type of transistor used in this circuit is the NPN transistor 2SCR542P from ROHM Semiconductors. The maximum rating for the collector-emitter voltage is 30 V and the collector current is 5 A. The turn-on voltage of this device or also called the collector-emitter saturation voltage is 0.4 V.

For the biasing circuit, we chose to bias the circuit at point A (the input bias voltage at the base) as 0.55 V with the DC supply voltage V1 as 20 V. Therefore, as shown in Fig. 2., the value of R3 is chosen to be 100 Ω and R2 to be 3.64 kΩ. The same voltage divider circuit is used for the other identical NPN transistor, i.e., R3 = R4 and R4 = R5.

When these voltage divider circuits are used, the input AC signal at the bases will shift up from the 0.53 V DC line (originally was 0.55 V but due to simulation adjustment, the DC value is 0.53 V). It should be noted that when the AC signal is connected to the voltage divider circuit it will drop slightly at point A. So, the signal will become a 4.86 Vpp AC signal. Finally, with the bias voltage, the positive peak becomes (4.86 + 0.53) 5.4 V and the negative peak becomes (-4.86 + 0.53) -4.3 V which is shown in Fig. 3. It should be
noted that the biasing is needed to be done closely to 0.55 V because if the biasing voltage chosen is more than 0.55 V, the conduction angle becomes more than 180 degrees. Conversely, if it is less than 0.55 V, the conduction angle reduces to less than 180 degrees.

Finally, two shunt capacitors are added at the emitter outputs which will control the upper cut-off points of the bandwidth.

**Fig. 3.** The effect of the voltage divider circuit on the input AC signal

The input signal shown in Fig. 3 is for the case of the Q1 transistor. For the Q2 transistor, the input will be the same but 180 degrees phase-shifted. However, the output of the entire circuit which is the combination of the emitter outputs of the transistors is shown in Fig. 4. The Q1 transistor is responsible for the odd numbered positive cycles at the output and the Q2 transistor for the even numbered positive cycles at the output.

**Fig. 4.** The pulsating DC output of the entire circuit.

**B. Combiner**

In the totem pole configuration, the combiner at the output is a center tapped step-up RF broadband transformer. The center tap is used to generate the phase shifted output of the Q2 transistor. The step-up voltage transformation ratio is used to ease up the requirement of the tracking signal for the envelope amplifier. Moreover, since the step-up operation affects the amplitude of the output voltage swing, it directly influences the efficiency of the amplifier. The overall circuit of the amplifier with the combiner is shown in Fig. 5 and the corresponding output signal shown in Fig. 6.

Two series capacitors (C1 and C2) are added at the outputs of the first phase shifter transformer to improve the linearity of the amplifier. In addition, these capacitors will control the lower cut-off point of the amplifier bandwidth.

**Fig. 5.** The overall circuit of the amplifier with the combiner

**Fig. 6.** The effect of capacitor on the linearity of the final amplifier output

**III. RESULTS AND DISCUSSION**

In this section, the calculation of efficiency is given. The dependency of efficiency on the transformer ratio is also discussed. The bandwidth of the overall simulated circuit is observed and presented. The dependency of bandwidth with coupling and bypass capacitances are also discussed in this section.

**A. Efficiency**

Theoretically, the efficiency, $\eta$ of the class B amplifier can be written as:

$$\eta = \frac{\pi}{4}(V_{output\_max} / V_1)$$

Where, $V_{output\_max}$ is the peak value of the output swing and $V_1$ is the fixed DC value of the DC voltage supply.

The circuit is built and simulated using LTSpice version XVII. From the equation it is clear that, when the value of $V_{output\_max}$ is equal to $V_1$ the efficiency is 78.5% which is maximum for a common collector amplifier in push-pull configuration since the maximum voltage gain is one. Whereas in totem pole configuration, the value of $V_{output\_max}$ is controlled by the turn ratio of the output combiner transformer. So, in this case the efficiency can be greater than 78.5%. But if the input AC signal level is low
then the transformer turn ratio needs to be very high to achieve a good efficiency. For an input of 5 Vpp sinusoidal signal, the effect of transformer ratio on the efficiency is listed below:

### Table I. TURN RATIO VS EFFICIENCY (5 Vpp)

<table>
<thead>
<tr>
<th>Turn ratio</th>
<th>( V_{\text{output-max}} ) (Volts)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:2</td>
<td>6.7</td>
<td>26.3</td>
</tr>
<tr>
<td>1:6</td>
<td>11.54</td>
<td>45.3</td>
</tr>
<tr>
<td>1:10</td>
<td>14.86</td>
<td>58.4</td>
</tr>
<tr>
<td>1:14</td>
<td>17.53</td>
<td>68.84</td>
</tr>
<tr>
<td>1:18</td>
<td>19.82</td>
<td>77.83</td>
</tr>
<tr>
<td>1:22</td>
<td>21.85</td>
<td>85.8</td>
</tr>
</tbody>
</table>

So, a transformer turn ratio of 1:18, which is very high, is needed to achieve an efficiency near to 78.5%. This high ratio can result in high heat loss as well as critical dimension problem of the device. A good trade off can be achieved if the input AC signal level is chosen to be half of the maximum DC voltage level. Suppose if an AC signal of 10 Vpp is used, then a low transformer ratio will result in high efficiency which is listed in the table below:

### Table II. TURN RATIO VS EFFICIENCY (10 Vpp)

<table>
<thead>
<tr>
<th>Turn ratio</th>
<th>( V_{\text{output-max}} ) (Volts)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:2</td>
<td>12.85</td>
<td>50.46</td>
</tr>
<tr>
<td>1:3</td>
<td>15.72</td>
<td>61.73</td>
</tr>
<tr>
<td>1:4</td>
<td>18.14</td>
<td>71.23</td>
</tr>
<tr>
<td>1:5</td>
<td>20.26</td>
<td>79.56</td>
</tr>
<tr>
<td>1:6</td>
<td>22.18</td>
<td>87.1</td>
</tr>
</tbody>
</table>

B. Bandwidth

![Fig. 7. The effect of coupling capacitors on bandwidth](image)

![Fig. 8. The effect of bypass capacitors on bandwidth](image)

The 3dB simulated bandwidth of the circuit is observed by doing an AC analysis in LTSpice. The bandwidth is recorded to be almost 80 MHz starting from 180 Hz to 80 MHz. A parametric analysis is done at the input coupling capacitor to see its effect on bandwidth. It is found that, by reducing the value of the capacitor will shift the lower cut-off frequency to the higher frequency region as shown in Fig. 7. On the other hand, increasing the value of the bypass capacitor shifts the upper cut-off frequency to the lower frequency region as shown in Fig. 8.

### IV. CONCLUSION

An efficient common collector class B amplifier is designed for the AET supply modulator application. The totem pole configuration is used so that the transistor pair used can be of the same type. A good trade off can be achieved between the transformer turn ratio and efficiency by selecting the value of the input AC signal almost half of the fixed DC voltage. For a 10 Vpp input AC signal, a turn ratio of 1:6 of the combiner transformer gives an efficiency of about 87%. The simulated bandwidth is recorded to have 80 MHz. The coupling and bypass capacitors help in improving the linearity of the amplifier and affects the bandwidth as well. The designed amplifier is suitable for the AET supply modulator used in the cellular base station applications.

### ACKNOWLEDGMENT

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