Comprehensive Analysis of Gate Oxide Short in Junctionless Fin Field Effect Transistor

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Abstract—Junctionless (JL) FinFET is one of the most promising alternatives to FinFET and planar MOSFET for future performance enhancements. The complexity of the JL FinFET manufacturing process has prompted difficulties in reliable device testing. Gate oxide short (GOS) is one of the most common faults that substantially influence circuit reliability, specifically in FinFET device structure. In this work, GOS defect model is presented for both n-channel and p-channel JL FinFET and JL FinFET-based inverter by introducing the defect as a pinhole designated by small cuboid cuts of different sizes for several coordination in the dielectric and filled with gate material. The electrical characteristics of 15nm n- and p-channel JL FinFET with fin height and width of 10nm, source/drain, channel and substrate doping concentration of 1.5x10^19 cm^-3, and work function of 4.76eV and 4.52eV for n- and p-channel are successfully simulated by using Synopsys Sentaurus TCAD Tools where Vth, SS, and DIBL are 0.371V, 75.7mV/dec and 42.7mV for n-channel and 0.3298V, 79.1mV/dec and 48.9mV for p-channel JL FinFET respectively that is compared with post GOS defect injection. The high-to-low delay time (tHL) is 1.61ps and low-to-high delay time (tLH) is 1.74ps for the defect-free inverter that is compared to the defected one where the tHL is 16.1% and tLH is 22.4% smaller than defective inverter. The findings of this research potentially result in the formation of a realistic analytical GOS fault model for circuit-level modeling.

Keywords—FinFET, junctionless, Gate oxide short, defect, pinhole, leakage

I. INTRODUCTION

The channel lengths of conventional field-effect transistors (FETs) are shrinking on the nanometer scale, posing several issues, including the requirement to minimize short channel effect, produce higher saturation current, and lower power consumption [1]. In the last decade, a various technique to overcome these obstacles have been proposed. For example, the direct tunnelling current in gate oxide can be suppressed using high-k/metal-gate technology, while short channel effects can be reduced by using multigate structures like FinFET and nanowires [2]-[3]. The junctionless (JL) FinFET containing the same doping concentration in source, drain, and channel is investigated, which has less leakage current, and a higher on/off current ratio compared to traditional FETs [4]-[5].

JL FinFET acts like a gated resistor with a gate that controls the carrier density and hence the current flow where the channel is vertically extended outside the substrate. JL FinFET is better for the avoidance of an ultrashallow source/drain junction, which simplifies the process flow. As well, the current transports through the bulk of the semiconductor, which lessens the effect of the imperfect semiconductor/insulator interfaces [6]. Consequently, the JL FinFET could be a potential structure for future silicon-based transistors.

Having a complex manufacturing process, the JL FinFET has caused new challenges regarding the appearance of new types of defects. Gate oxide short (GOS) defect is one of the dominant defects due to the continual reduction in transistor size and dielectric thickness, that is occurred because of airborne particles, mask damages, and over-etching of the poly-Si gate, resulting in a direct current path between the gate and the channel [7]. To accurately model GOS defects, the behavior of the JL FinFET device is needed to be comprehensively investigated. GOS defects in JL FinFET have been researched in a few studies. The drain current is negative at low drain bias, and the saturation current is lower in a defective FinFET than in a defect-free FinFET [8]. The results will help to develop more practical logic circuits or inverters.

In this paper, the device and circuit performances of JL FinFET are thoroughly investigated. Furthermore, using Synopsys’ Sentaurus TCAD tool, the GOS defect in JL FinFET has been analyzed by examining faulty device performance at different locations and sizes of the cuboid cuts ranging in size from 2nmx2nm to 4nmx4nm in the gate oxide. The pinholes in the gate oxide are placed around the drain, source, and center of the gate. In Section II, the methodology and simulation setup are introduced. The effects of the defective JL FinFET structures are shown in Section III. The conclusion is summarized in Section IV.

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II. SIMULATION

A. Junctionless FinFET

A 15 nm n-channel JL FinFET is designed using Sentaurus TCAD with the appropriate device parameter shown in Fig. 1. In this research, 15 nm of gate length, 10 nm of width and height of fin, and 1 nm gate oxide thickness are used to design the device shown in TABLE I. For 15 nm p-channel JL FinFET, same physical parameters are used.

![Fig. 1. Device structure of junctionless FinFET](image)

**TABLE I. PHYSICAL PARAMETER USED FOR JUNCTIONLESS N-CHANNEL FINFET**

<table>
<thead>
<tr>
<th>Device Parameters</th>
<th>This work</th>
<th>[6]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fin Width ($W_{fin}$)</td>
<td>10nm</td>
<td>10nm</td>
</tr>
<tr>
<td>Fin Height ($H_{fin}$)</td>
<td>10nm</td>
<td>10nm</td>
</tr>
<tr>
<td>Gate Length ($L_g$)</td>
<td>15nm</td>
<td>15nm</td>
</tr>
<tr>
<td>Gate oxide thickness ($T_{ox}$)</td>
<td>1nm</td>
<td>1nm</td>
</tr>
<tr>
<td>Doping concentration of Channel, Substrate</td>
<td>$1.5 \times 10^{19}$ cm$^{-3}$</td>
<td>$1.5 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Material</td>
<td>Silicon</td>
<td>Silicon</td>
</tr>
<tr>
<td>Gate oxide</td>
<td>HfO$_2$</td>
<td>HfO$_2$</td>
</tr>
</tbody>
</table>

B. Junctionless FinFET based Inverter

An inverter for 15 nm junctionless FinFET is designed by using Sentaurus TCAD with the appropriate device parameter shown in Fig. 2. To achieve symmetry, the nFET and pFET IV curves must be matched while being folded [9].

C. Defect injection in Single channel FinFET

After successfully designing the 15 nm n-channel junctionless FinFET using Sentaurus TCAD, a pinhole is introduced in gate oxide in different sizes for several coordination near the source, drain, and at the middle of the gate in gate oxide, which is shown in Fig. 3. The pinhole is filled with gate material which is silicon [10]. The reason for choosing these specific positions as it will be easy to characterize the behavior of the defect injection.

![Fig. 3. Junctionless n-channel FinFET with defect injection in gate Oxide](image)

D. Defect injection in Inverter

The ratio of $W_p$ to $W_n$ is typically about three to account for the ratio in 15nm JL FinFET [9]. After successfully designing an inverter for junctionless FinFET using Sentaurus TCAD, pinholes of various sizes are put into the gate oxide for multiple coordination. In Fig. 4, pinhole is introduced near the source of the gate oxide.

![Fig. 4. Inverter with larger defect injection in different locations of gate oxide](image)
III. RESULT AND DISCUSSION

A. Electrical Characteristics of JL FinFET

From the $I_d-V_g$ graph (linear scale), the threshold voltage is 0.3712V and 0.3293V, DIBL is around 42.7 mV/V and 48.9 mV/V for n-channel and p-channel respectively. Regarding the $I_d-V_g$ graph (log scale), the subthreshold swing is approximately 75.7 mV/dec and 79.1 mV/dec for n-channel and p-channel respectively. Fig. 5. shows the plots of the $I_d-V_g$ curves of the 15nm n-type and p-type devices. To ensure a fair comparison, linear threshold voltages ($V_{th}$) are tuned to around 300 mV and the electrical properties have been validated with this work [6].

![Fig. 5. $I_d-V_g$ curves of 15nm n-type and p-type junctionless FinFET](image)

The threshold voltage ($V_{th}$) for both n- and p-channel is increased due to the size of the defect injection in the gate oxide. For the saturation region, the $V_{th}$ is 0.3712V, 0.42451V and 0.42528V for defect-free, 2nm x 2nm and 4nm x 4nm sizes of pinhole injected JL FinFET respectively.

In Fig. 6, the I-V Graph of n channel JL FinFET for $V_{ds}=0.05V$ for different sizes and locations of the pinhole is shown. At the linear region, the defect-free drain current is higher compared to the defective ones. A pinhole close to the source has the highest current density of electrons flowing from the drain at low drain voltage, resulting in a higher negative drain current [10].

![Fig. 6. I-V Graph of n channel JL FinFET for $V_{ds}=0.05V$ for different size and location of pinhole](image)

The drain currents for all situations are quite near at saturating bias shown in Fig. 7. A pinhole near the drain produces the maximum drain current under the strong electric field around the drain region.

The Saturation current of defect-free will be higher than the defected ones, which is 15.7 µA. The saturation current decreases as the pinhole become larger. 4nm x 4nm larger pinhole applied near the source produces the lowest saturation current which is 8.79 µA shown in Fig. 8. The saturation current does not alter significantly with the position of the defects.

![Fig. 7. I-V Graph of n-channel JL FinFET for $V_{ds}=1V$ for different size and location of pinhole](image)

![Fig. 8. Saturation current of n-channel JL FinFET with and without defect](image)

![Fig. 9. Leakage currents of n-channel JL FinFET with and without defect](image)
Leakage current will be increased due to the increment of the size of the pinhole [10]. According to the size and position, the non-defective leakage current will be smaller than defected leakage current. In Fig. 9, the leakage current is higher when a 4nm×4nm pinhole is injected near the source which is 67.9 pA. The lowest leakage current is 52.8 pA when no pinhole is injected into the dielectric.

For p-channel, the I-V curve is also aligned and validated with the n-channel JL FinFET of this work [6]. The highest saturation current is 12.27 µA, and the lowest leakage current is 156.5 pA when no pinhole is injected into the dielectric for p-channel device. On the hand, the lowest saturation current is 7.31 µA and the highest leakage current is 191.67 pA when a 4nm×4nm pinhole is injected near the source in the dielectric for p-channel JL FinFET.

B. Inverter

In Fig. 10, the defective inverter voltage-time curve of $L_g=15$ nm JL FinFET is shown where the propagation delay can be observed.

![Fig. 10. Inverter voltage-time curve of $L_g=15$ nm JL FinFET with defects in different positions.](image)

The high to low delay time ($t_{HL}$) is usually smaller than low to high delay time ($t_{LH}$) shown in TABLE II.

<table>
<thead>
<tr>
<th></th>
<th>Defect Free</th>
<th>Defect near Drain</th>
<th>Defect near Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-to-low delay time ($t_{HL}$)</td>
<td>1.61 ps</td>
<td>1.87 ps</td>
<td>1.81 ps</td>
</tr>
<tr>
<td>Low-to-high delay time ($t_{LH}$)</td>
<td>1.74 ps</td>
<td>2.13 ps</td>
<td>2.21 ps</td>
</tr>
</tbody>
</table>

The n-type device starts to turn on when the input signal transitions from low to high voltage; thus, the $t_{HL}$ is dependent on the threshold voltage. When the input signal changes from high to low voltage, the p-type device begins to turn on, that is why $t_{LH}$ is dependent on the threshold voltage. The $t_{HL}$ and $t_{LH}$ are higher in defective devices because the threshold voltage for n- and p-type devices are higher in defective devices compared to defect-free device.

IV. CONCLUSION

The JL FinFET has a higher ON-OFF current ratio and improved short channel properties according to the device simulations of electrical characteristics. The inverter made by JL FinFET had better timing and static transfer characteristics regarding the circuit performance. The impact of the GOS defect on JL FinFET electrical characteristics is investigated for several locations and sizes. After comparing before and after GOS defect injection, it is noticeable that the threshold voltage is increased after defect injection. At linear bias condition, a pinhole close to the source has a larger negative drain current, and at saturation bias condition, a pinhole close to the drain results in the highest drain current. The saturation current of defect-free is 44.1% and 40.4% higher and the leakage current of defect-free is 28.6% and 22.5% lower than 4nm×4nm size of pinhole injected n- and p-channel JL FinFET respectively. In addition, the delay time $t_{HL}$ for defect-free inverter are 16.1% and 12.4% smaller and $t_{LH}$ are 22.4% and 27.1% smaller than defective inverter where pinhole is injected near drain and source respectively. The simulation results can be applied to develop analytical GOS fault models.

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